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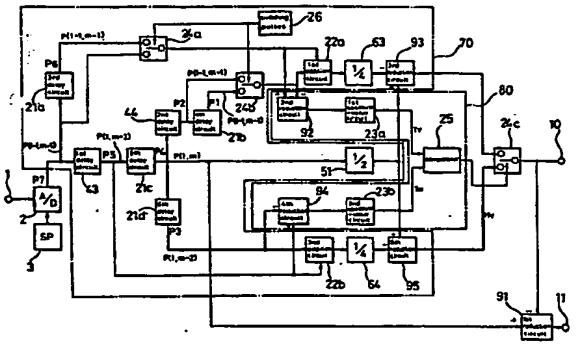
(54) **A separating filter of luminance and chrominance signals of pal system.**

(57) A filter for separating luminance and chrominance signals from the composite television signals of PAL system, comprising: a sampling signal generator for generating a sampling signal having a frequency of four times that of color sub-carrier wave, and whose phase is in accordance with the U and V axis of the chrominance signal; and A/D converter for converting the input analog composite television signals into digital signals with the use of the sampling signal; a vertical and a horizontal filter for separating a chrominance signal at each particular sampling point, with the use of a sample value obtained at each sampling point through the A/D conversion, the sample values of first adjacent sampling points adjacent to each particular point, wherein the first adjacent points have a reversed color sub-carrier wave phase to that of each particular point, and wherein the first adjacent point are one line up or below of each particular point, or of second adjacent points on the same line as that of each particular point, wherein the second adjacent points have a reversed color sub-carrier wave phase to that of each particular point; a detecting means for detecting a direction in which the signal has less variation, with the use of the sample values of the first and second adjacent sampling points; a selecting means for selecting either output of the vertical or horizontal filter in the direction detected by the detecting means; and a luminance signal generator for outputting luminance signals by separating chrominance signals from the digitized composite television signals.



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# A separating filter of luminance and chrominance signals of PAL system

## FIELD OF THE INVENTION

The present invention relates to a filter for separating luminance signals and chrominance signals (hereinafter referred to as the YC separating filter) whereby the luminance signals (hereinafter referred to as the Y signals) and the chrominance signals (hereinafter referred to as the C signals) are separated and extracted from composite television signals (composite video signals) of a PAL system (phase alternative by line color system). More particularly, the present invention relates to a system under which the analog composite television signals of PAL system are converted into digital signals, which are subsequently separated into Y and C signals.

## BACKGROUND OF THE INVENTION

Under the current standard color television system the Y and C signals are transmitted as frequency-multiplexed composite signals. Accordingly it is required for the receivers to separate the Y and C signals distinctly from the composite signals received thereat.

The composite television signals P of PAL system consists of the Y signal, and the C signal which is

produced by executing a quadrature two-phase modulation to two color difference signals U and V (alternatively, I and Q) by a color sub-carrier frequency fsc. The P is expressed as follows:

$$P = Y + C$$
$$= Y + U \cdot \sin(2\pi fsc\ t) \pm V\cos(2\pi fsc\ t)$$

where the $\pm$ means the "+" for the odd scanning lines and the "-" for the even scanning lines. This means that the V components are reversed in every scanning line. Suppose that the frame frequency be fF (25Hz), the field frequency fV (50Hz), the horizontal scanning frequency be fH (15.625KHz), the following relationship is established between these and the above-mentioned fsc:

$$fsc = (284 - 1/4 + 1/625)\ fH$$
$$= (284 - 1/4 + 1/625)\ 625 \cdot fV/2$$
$$= (284 - 1/4 + 1/625)\ 625fF$$

It will be understood from this relationship that the fsc and fH are in the 1/4 line off-set relationships. For this reason a sample signal series obtained from the composite television signals of PAL system being synchronuously sampled with a sampling frequency fs of four times the color sub-carrier frequency is represented in a two-dimensional array on the screen as shown in Figure 1. It will be understood from Figure 1

that the phases of the color signals are repeated at each of four lines. In Figure 1 the rectangles, circles and triangles show sampling points Ps, and the Y shows luminance signals, and the C1, C2, C1', and C2' show color signals, the U1, U2, V1 and V2 show color difference signals, respectively.

In order to secure the compatibility with monochrome television signals, it is required that the receivers can separate Y and C signals exactly from the composite color television signals containing C signals which are frequency-multiplexed in such a manner that the spectrum frequency-interleaves in the frequency band of the Y signals.

Figure 2 shows an example of the known Y-C separating filter:

There are provided an input terminal 1 for analog composite television signals of PAL system, and A/D converter 2, a sampling pulse generator (SP) 3, and first and second delay circuits 41 and 42 (two line memory) for delaying the sampling signals from the A/D converters two horizontal scanning periods. The reference numerals 5, 61 and 62, and 7 designate a 1/2 times multiplication circuit, first and second 1/4 times multiplication circuits, and a reduction circuit, respectively. The last-mentioned reduction circuit 7

is designed to reduce the output of the first and second 1/4 times multiplication circuits 61 and 62 from that of the circuit 5. The reference numerals 8 and 9 designate a horizontal band-pass filter, and a second reduction circuit, respectively, the latter being designed to reduce the output of the filter 8 from the output of the first delay circuit 41. The reference numeral 10 designates an output terminal of the horizontal band-pass filter 8, and the numeral 11 designates an output terminal of the second reduction circuit 9. The circuit of Figure 2 is operated as follows:

The sampling pulse generator 3 is an oscillator which synchronuously oscillates at a frequency fs of four times the color sub-carrier frequency fsc of the composite television signals which are applied to the input terminal 1. The output of the generator 3 is applied to the A/D converter 2, in response to which the A/D converter digitizes the analog signals applied to the input terminal 1. The sampled signal series which are obtained by sampling the composite color television signals of PAL system at the sampling frequency: fs = 4fsc, show the patterns on the screen shown in Figure 1 when the phases of C signals are noted. As evident from Figure 1, the phase of C

signals periodically changes in a period of four lines, it will be understood that the phase of the color sub-carrier of its chrominance signal component is reversed 180° on the lines ($\ell$-2) and ($\ell$+2) two lines up and below of the line ($\ell$). The 1/2 times circuit 5 multiplies the output of the 1st delay circuit 41 1/2 times, the output of which is spplied to the reduction circuit 7. The 1st 1/4 times circuit 61 multiplies the output of the A/D converter 2 1/4 times, the output of which is applied to the reduction circuit 7. The 2nd 1/4 times circuit 62 multiplies the output of the 2nd delay circuit 42 1/4 times, the output of which is applied to the reduction circuit 7. The reduction circuit 7 reduces the outputs of the 1st 1/4 times circuit 61 and the 2nd 1/4 times circuit 62 from that of the 1/2 times circuit 5. Therefore, the output of the reduction circuit 7 Hc ($\ell$, m) is expressed by:

$$Hc(\ell, m) = 1/4\{-P(\ell-2, m) + 2P(\ell, m) - P(\ell+2, m)\}$$

where the P($\ell$, m) is the sample value at the (m)th sampling point on the ($\ell$)th line, and the P($\ell$+2, m) is a sample signal, which is the output of the A/D converter 2. The P($\ell$, m) is the signal to be separated, which is the output of the 1st delay circuit 41. The P($\ell$-2, m) is a sample signal which is the

output of the 2nd delay circuit 42. The output signal of the reduction circuit 7 $Hc(\ell, m)$ is applied to the horizontal band-pass filter 8, which is a filter adapted to pass the chrominance signal component and to remove the Y signal component in the output signal $Hc(\ell, m)$. This filter can be constructed on the following formula:

$$Hh(Z) = -1/32 \cdot (1 - z^{-2})^2 (1 + z^{-4})^2 (1 + z^{-8})$$

It will be understood from the formula that the C signal is obtained from the output of the horizontal band-pass filter 8.

The reduction circuit 9 reduces the output of the horizontal band-pass filter 8 from that of the 1st delay circuit 41, which means that the circuit 9 reduces the chrominance signal (C) from the composite television signal (P). Thus the Y signal is obtained in the output of the reduction circit 9. The output terminals 10 and 11 are connected to the horizontal band-pass filter 8, and the reduction circuit 9, respectively, from which it will be understood that the C signal is obtained at the terminal 10, and that the Y signal is obtained at the terminal 11.

As evident from the foregoing description, the conventional filter for separating the Y- and C-signals

comprises a combination of a horizontal and vertical filters fixed together. In addition, the conventional system is on the presumption that the picture elements as the sample value series of television signals which are adjacent to each other on the screen are similar with each other. Consequently, in an area where the luminance and chrominance of picture rapidly change, the Y signal and C signal are likely to leak into each channel, thereby causing cross-color and cross-luminance distortion. This spoils the quality of the reproduction of pictures.

OBJECTS AND SUMMARY OF THE INVENTION

The present invention is directed to overcome the problems pointed out above, and has for its object to provide a YC separating filter of PAL system wherein the input composite color television signals are converted into digital signals by sampling signals having a frequency of four times the color sub-carrier frequency, and the luminance signals and chrominance signals are separated from each other, which secures an exact separation with the use of a one-line memory and without the use of a two-line memory.

Other objects and advantages of the present invention will become apparent from the detailed description given hereinafter; it should be understood,

however, that the detailed description and specific embodiment are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

According to the present invention, there is provided a filter for separating luminance and chrominance signals from the composite television signals of PAL system, comprising: a sampling signal generator for generating a sampling signal having a frequency of four times that of color sub-carrier wave, and whose phase is in accordance with the U and V axis of the chrominance signal; an A/D converter for converting the input analog composite television signals into digital signals with the use of the sampling signal; a vertical and a horizontal filter for separating a chrominance signal at each particular sampling point, with the use of sample value obtained at each sampling point through the A/D conversion, the sample values of first adjacent sampling pionts adjacent to each particular point, wherein the first adjacent points have a reversed color sub-carrier wave phase to that of each particular point, and wherein the first adjacent points are one line up or below of each particular point, or of second adjacent points on the

same line as that of each particular point, wherein the second adjacent points have a reversed color sub-carrier wave phase to that of each particular point; a detecting means for detecting a direction in which the signal has less variation, with the use of the sample values of the first and second adjacent sampling points; a selecting means for selecting either output of the vertical or horizontal filter in the direction detected by the detecting means; a luminance signal generator for outputting luminance signals by separating chrominance signals from the digitaized compsite television signals.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a diagrammatic view showing series of sample signals obtained by sampling the composite television video signals of PAL system at a sampling frequency of four times that of the color sub-carrier wave;

Figure 2 is a circuit diagram showing a conventional filter for separating luminance and chrominance signals;

Figure 3 is a circuit diagram showing a filter of one embodiment of the present invention;

Figure 4 is a diagrammatic view showing series of sample signals obtained when the composite television

video signals of PAL system are sampled under the present invention;

Figures 5 and 6 are diagrammatic views each showing the operation of the filter shown in Figure 3;

Figure 7 is a circuit diagram showing a modified version of the embodiment;

Figure 8 is a diagrammatic view showing series of sample signals obtained in the modified version of Figure 7; and

Figures 9 and 10 are diagrammatic views each showing the operation of the filter shown in Figure 7.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Figure 3, the reference numerals 1 and 3 designate an input terminal for receiving composite color television signals in analog form, which contain Y and C signals, and a sampling signal generator which comprises a sampling pulse generating circuit (SP), respectively. The reference numeral 2 designates an A/D converter for converting the composite color television signals in analog form into digital signals by the sampling signals from the sampling signal generator 3. The reference numerals 43 and 44 designate first and second delay circuits (one line memory) designed to delay the signals received thereat by a shorter period of time by one sampling

period than one horizontal scanning period. The reference numerals 21a, 21b, 21c and 21d designate third, fourth, fifth and sixth delay circuits designed to delay the signals received thereat by two sampling periods. A sample signal generator is constituted by these 1st to 6th delay circuits, which generator outputs the signal to be separated and 1st to 6th sample signals on the basis of the digital signals from the A/D converter 2. The signal to be separated P ($\ell$, m) is a signal output from the 5 th delay circuit 21c, the 1st sample signal P ($\ell$-1, m-1) is output from the 4th delay circuit 21b, and is a signal delayed a longer period of time by one sampling period than one horizontal scanning period as compared with the signal to be separated, the 2nd sample signal P ($\ell$-1, m+1) is output from the 2nd delay circuit 44, and is a signal delayed a longer period of time by one sampling period than one horizontal scanning period as compared with the signal to be separated, the 3rd sample signal P ($\ell$, m-2) is output from the 6th delay circuit 21d, and is a signal delayed two sampling periods as compared with the signal to be separated, the 4th sample signal P ($\ell$, m+2) is output from the 1st delay circuit 43, and is a signal advanced two sampling periods as compared with the signal to be separated, the 5th sample signal P ($\ell$

+1, m-1) is output from the 3rd delay circuit 21a, and is a signal advanced a shorter period of time by one sampling period than one horizontal scanning period as compared with the signal to be separated, the 6th sample signal P ($\ell$+1, m+1) is output from the A/D converter 2, and is a signal advanced a longer period of time by one sampling period than one horizontal scanning period as compared with the signal to be separated. The reference numeral 26 designates a switching pulse generator which outputs first and second state signals having "H" level and "L" level, respectively. The reference numeral 24a designates a second switching circuit which, receiving the 5th and 6th sample signals from the 3rd delay circuit 21a and from the A/D converter 2, respectively, selectively outputs the 5th sample signal in response to the 1st state signal from the switching signal generator 26, and the 6th smaple signal in response to the second state signal. The reference numeral 24b designates a first switching circuit which, receiving the 2nd sample signal from the 2nd delay circuit 44 and the 1st sample signal from the 4th delay circuit 21b, selectively outputs the 2nd sample signals in response to the 1st state signal from the switching signal generator 26, and the 1st sample signal in response to the 2nd state

signal. The reference numeral 92 designates a second reduction circuit which outputs a difference signal between the selected output from the 1st switching circuit 24b and the selected output from the 2nd switching circuit 24a. The reference numeral 23a designates a 1st absolute-value circuit which outputs the absolute value of the difference signal from the 2nd reduction circuit 92 as Tv signal. This circuit 23a constitutes a Tv signal generator with the 2nd reduction circuit 92.

The reference numeral 94 designates a 4th reduction circuit which outputs a difference signal between the 4th sample signal from the 1st delay circuit 43 and the 3rd sample signal from the 6th delay circuit 21d, and the reference numeral 23b designates a 2nd absolute-value circuit which outputs the absolute value of the difference signal from the 4th reduction circuit 94 as $T_H$ signal, which constitutes a $T_H$ signal generator with the 4th reduction circuit 94. The reference numeral 25 designates a comparator which compares between the Tv signal from the 1st absolute-value circuit 23a and the $T_H$ signal from the 2nd absolute-value circuit 23b, and outputs a first state signal when the Tv is smaller than the $T_H$, whereas it outputs a second state signal when the $T_H$ is

smaller than the Tv. The Tv signal generator, the $T_H$ signal generator and the comparator 25 constitute a detector circuit 80 which detects a direction in which the composite television signals have less variation. The reference numeral 22a designates a first addition circuit which outputs the sum of the selected output from the 1st switching circuit 24b and that from the 2nd switching circuit 24a. The reference numeral 63 designates a first multiplication circuit which multiplies the output of the first addition circuit 22a 1/4 times. The reference numeral 51 designates a third multiplication circuit which multiplies the signal to be separated from the 5th delay circuit 21c. The reference numeral 93 designates a third reduction circuit which outputs a difference signal between the output signal from the 3rd multiplication circuit 51 and that from the 1st multiplication circuit 63 as Hc signal which is a chrominance signal in the horizontal direction. This circuit 93 constitutes a Hc signal generator in combination with the 1st addition circuit 22a, the 1st multiplication circuit 63, and the 3rd multiplication circuit 51. The reference numeral 22b designates a second addition circuit which outputs the sum of the 4th sample signal from the 1st delay circuit 43 and the 3rd sample signal from the 6th delay circuit

21d. The reference numeral 64 designates a second multiplication circuit which multiplies the output of the second addition circuit 22b 1/4 times. The reference numeral 95 designates a fifth reduction circuit which outputs a difference signal between the output signal from the 3rd multiplication circuit 51 and that from the 2nd multiplication circuit 64 as chrominance signal Vc in the vertical direction. This circuit 95 constitutes a Vc signal generator in combination with the 2nd addition circuit 22b and the 2nd multiplication circuit 64. The sample signal generator, the Hc signal generator, and the Vc signal generator constitute a vertical-direction filter and a horizontal-direction filter 70. The reference numeral 24c designates a selecting device which, receiving the Hc signal from the 3rd reduction circuit 93 and the Hv signal from the 5th reduction circuit 95, and also receiving the first and second state signals from the comparator 25, selectively outputs the Hc signal as chrominance signal to an output terminal 10 for chrominance signal in response to the first state signal, and selectively outputs the Vc signal as chrominance signal to the output terminal 10 in response to the second state signal. The reference numeral 91 designates a first reduction circuit which

outputs a difference signal between the signal to be separated from the 5th delay circuit 21 and the chrominance signal of the selected output from the selecting device 24c to an output terminal for luminance signal as luminance signal 11.

The circuit shown in Figure 3 is operated as follows:

The sampling pulse generator 3 is an oscillator which synchronously oscillates at a frequency fs which is a frequency of four times the color sub-carrier wave frequency fsc for composite television signals which are applied to the input terminal 1. It is arranged so that the phase of the sampling pulse therefrom is in accordance with the axes (U and V axis) of the color difference signals (R-Y) and (B-Y). The sampling pulses output from the circuit 3 are applied to the A/D converter 2, in response to which the A/D converter converts the analog composite signals into digital ones. The composite color television signals of PAL system which have been sampled by the sampling pulses appear as shown in Figure 4 when the phase of C signal is noted.

Referring to Figure 5 and 6, the embodiment will be described in greater detail:

The illustrations in Figures 5 and 6 are basically

the same as that in Figure 4, except for the addition of reference signs and numerals. The case shown in Figure 5 is described in the following with the use of the circuit of Figure 3.

Suppose that the A/D converter 2 outputs a signal at P7 (the 6th sample signal) at a time T. Then the 3rd delay circuit 21a outputs a signal at P6 (the 5th sample signal); the 4th delay circuit 21b outputs a signal at P1 (the 1st sample signal); the 1st delay circuit 43 outputs a signal at P5 (the 4th sample signal); the 2nd delay circuit 44 outputs a signal at P2 (the 2nd sample signal); the 5th delay circuit 21c outputs a signal at P4 (the signal to be separated); and the 6th delay circuit 21d outputs a signal at P3 (the 3rd smaple signal). In this case, the point where the Y and C separation is to be carried out, that is, the signal to be separated is the P4.

Referring to Figure 5, the switching signal generator 26 sends a control signal to the 2nd switching circuit 24a, in such a manner as to allow the output signal from the 3rd delay circuit 21a to pass, and sends a control signal to the 1st switching circuit 24b to allow the output signal from the 2nd delay circuit 44 to pass.

In this way the output signal of the 2nd switching

circuit 24a becomes a sample value of the point P6, and likewise that of the 1st switching circuit 24b becomes a sample value of the point P2.

The 1st addition circuit 22a adds the output of the 2nd switching circuit 24a and that of the 1st switching circuit 24b, and the 1st multiplication circuit 63 multiplies the output of the addition circuit 22a 1/4 times. The 3rd multiplication circuit 51 multiplies the output of the 5th delay circuit 21c 1/2 times. The 3rd reduction circuit 93 reduces the output of the 1st multiplication circuit 63 from that of the 3rd multiplication circuit 51, and outputs a signal Hc which is expressed by:

$$-1/4\ (\text{the sample value at the point P6}) + 1/2\ (\text{the sample value at the point P4}) - 1/4\ (\text{the sample value at the point P2}).$$

The 2nd addition circuit 22b adds the output of the 1st delay circuit 43 and that of the 6th delay circuit 21d, and the 2nd multiplication circuit 64 multiplies the output of the addition circuit 22b 1/4 times. The 5th reduction circuit 95 reduces the output of the 2nd multiplication circuit 64 from the output of the 3rd multiplication circuit 51. In this way the output signal of the circuit 95, that is, Vc signal is expressed by:

- 1 / 4 (the sample value at the point P3)

+ 1 / 2 (the sample value at the point P4)

- 1 / 4 (the sample value at the point P5).

The outputs of the 2nd switching circuit 24a and the 1st switching circit 24b are applied to the 2nd reduction circuit 92, the output of which is taken an absolute value by the 1st absolute-value circuit 23a. Accordingly, the output signal Tv of the 1st absolute-value circuit 23a is:

$$Tv = |(\text{the sample value at the point P6}) - (\text{the sample value at the point P2})|$$

The outputs of the 1st delay circuit 43 and the 6th delay circuit 21d are applied to the 4th reduction circuit 94, the output of which is taken an absolute value by the absolute-value circuit 23b. The output signal of the 2nd absolute-value circuit 23b (TH) is expressed by:

$$TH = |(\text{the sample value at the point P5}) - (\text{the sample value at the point P3})|$$

The output signal Tv of the 1st absolute-value circuit 23a and the output signal TH of the 2nd absolute-value circuit 23b are added to the comparator 25, which compares them thereby to send a control signal from the 3rd reduction circuit 93 and from the 5th reduction circuit 95. When Tv is smaller than the

TH, the selecting circuit 24c outputs the 1st state signal so as to ensure that the output thereof becomes an output of the 3rd reduction circuit 93, whereas, when Tv is equal to or larger than TH, the selecting circuit 24c outputs the 2nd state signal so as to ensure that the output thereof becomes an output of the 5th reduction circuit 95.

Under the illustrated system the adjacent picture element signals whose phases of color sub-carrier waves are reversed with relative to that of the signal to be separated (the reversed sampling points) are used to detect a direction in which the signals have less variation, and the picture element signal in the detected direction is used to separate the C signals from the composite television signals. This system ensures an exact, clear separation.

At next, the case in Figure 6 is described in the following with the use of the circuit of Figure 3.

Suppose that the A/D converter 2 outputs a signal at P7 (the 6th sample signal) at a time T. The 3rd delay circuit 21a outputs a signal at P6 (the 5th sample signal); the 4th delay circuit 21b outputs a signal at P1 (the 1st sample signal); the 1st delay circuit 43 outputs a signal at P5 (the 4th sample signal); the 2nd delay circuit 44 outputs a signal at

P2 (the 2nd sample signal); the 5th delay circuit 21c outputs a signal at P4 (the signal to be separated); and the 6th delay circuit 21d outputs a signal at P3 (the 3rd sample signal).

In the embodiment shown in Figure 6 the switching signal generator 26 sends a control signal to the 2nd switching circuit 24a in such a manner as to allow the output signal of the A/D converter 2 to pass, and sends a control signal to the 1st switching circuit 24b in such a manner as to allow the output signal of the 4th delay circuit 21b to pass.

In this way the output of the 2nd switching circuit 24a becomes a sample value at the point P7, and that of the 1st switching circuit 24 becomes a sample value at the point P1.

The 1st addition circuit 22a adds the outputs of the 2nd switching circuit 24a and of the 1st switching circuit 24b, and the 1st multiplication circuit 63 multiplies the output of the circuit 22a 1/4 times. The 3rd multiplication circuit 51 multiplies the output of the 5th delay circuit 21c 1/2 times. The 3rd reduction circuit 93 reduces the output of the 1st multiplication circuit 63 from that of the 3rd multiplication circuit 51. In this way the output signal of this reduction circuit 93 (Hc) is expressed

by:

- 1 / 4 (the sample value at the point P7)
+ 1 / 2 (the sample value at the point P4)
- 1 / 4 (the sample value at the point P1)

The 2nd addition circuit 22b adds the outputs of the 1st delay circuit 43 and of the 6th delay circuit 21d, and the 2nd multiplication circuit 64 multiplies the output of this cirucit 22b 1/4 times. The 5th reduction circuit 95 reduces the output of the 2nd multiplication circuit 64 from that of the 3rd multiplication circuit 51. In this way the output signal of the reduction circuit 95 (Vc) is expressed by:

- 1 / 4 (the sample value at the point P3)
+ 1 / 2 (the sample value at the point P4)
- 1 / 4 (the sample value at the point P5)

The outputs of the 1st switching circuit 24a and the 2nd switching circuit 24b are applied to the 2nd reduction circuit 92', the output of which is taken an absolute value by the 1st absolute-value circuit 23a. Consequently, the output of the 1st absolute-value circuit 23a, that is, the signal TV, is expressed by:

Tv = |(the sample value at the point P7)
- (the sample value at the point P1)|

The outputs of the 1st delay circuit 43 and of the

6th delay circuit 21d are applied to the 4th reduction circuit 94, the output of which is taken an absolute value by the 2nd absolute-value circuit 23b. Consequently, the output of the 2nd absolute-value circuit 23b, that is, the signal TH, is expressed by:

$$TH = |(\text{the sample value at the point P5}) - (\text{the sample value at the point P3})|$$

The output Tv of the 1st absolute-value circuit 23a and the output TH of the 2nd absolute-value circuit 23b are applied to the comparator 25, which compares these outputs Tv and TH thereby to send a control signal of the 1st or 2nd state signal to the selecting circuit 24c. The selecting circuit 24c has already received the outputs of the 3rd reduction circuit 93 and the 5th reduction circit 95. When Tv is smaller than TH, the comparator 25 outputs the 1st state signal so that the output of the selecting circuit 24c becomes that of the 3rd reduction circuit 93. When Tv is equal to, or larger than TH, the comparator 25 outputs the 2nd state signal to the selecting circuit 24c so that the output of the selecting circuit 24c becomes that of the 5th reduction cirucit 95.

Under the illustrated system the adjacent picture element signals whose color sub-carrier wave phases are reversed with relative to that of the signal to be

separated are used to detect a direction in which the signals have less variation, and the picture elements in the detected direction are used to separate the C signals from the composite television signals. Thus the system ensures an exact, clear separation.

The operation of the switching signal generator 26 will be described:

As evident from Figure 3, let us note some particular point, for example, the point P4. Sampling points whose color sub-carrier wave phases are reversed with relative to that of the signal to be separated at point P4 are found two points forward or backward on the same line, and on the upper and lower lines there are two cases, that is:

(1) one sampling point backward of the sampling point one line up, and one sampling point forward of the sampling point one line below; and

(2) one sampling point forward of the sampling point one line up, and one sampling point backward of the sampling point one line below..

The cases (1) and (2) have been described with reference to Figures 5 and 6, respectively. To embody a Y- and C-signals separating filter, it is required to ascertain which case of the Figures 5 and 6 the arrangement of the adjacent sampling points belong to,

and send a control signal to the 2nd or 1st switching circuit 24a or 24b, respectively. For example, in Figures 5 and 6 the absolute value of the difference signal between the sample value at the point P4 (the signal to be separated) and that at the point P1, and the absolute value of the difference between the sample value at the point P4 and that at the point P2 are compared.

$$\left|(\text{the sample value at the point P4}) - (\text{the sample value at the point P1})\right| < \left|(\text{the sample value at the point P4}) - (\text{the sample value at the point P2})\right|$$

When this relationship is established, the switching signal generator 26 outputs a control signal in such a manner as to allow the 2nd switching circuit 24a to pass the output signal of the 3rd delay circuit 21a, and to allow the 1st switcing circuit 24b to pass the output signal of the 2nd delay circuit 44.

When the relationship is opposite, the switching signal generator 26 outputs a control signal in such a manner as to allow the 2nd switching circuit 24a to pass the output signal of the A/D converter 2, and to allow the 1st switching circuit 24b to pass the output signal of the 4th delay circuit 21b.

For example, when the phase of the sampling signal

is fixed, the two-dimensional arrangement shown in Figure 4 is fixed. Accordingly, the generator 26 can be constructed so that the 2nd and 1st switching circuits 24a, 24b are switched at every sampling point on each line through the recognition of horizontal lines of the input signals at the terminal 1.

The 1st reduction circuit 91 reduces the output of the switching circuit 24c from that of the 5th delay circuit 21c, the latter output being a composite television signal, and the output signal of the selecting cirucit 24c being a C-signal separated from the composite television signal. As a result, the output of the 1st reduction circuit 91 becomes a Y-signal.

Under the above-mentioned system the sample values at points one line up and below or alternatively the smaple values at points two points forward and backward on the same line with relative to a specific sampling point are used to effect the separation of Y and C signals. Since the used sample values have little variation, the exact and clear separation is secured as compared with the conventional separating system. In addition, the values of the adjacent sampling points are used to detect a direction in which the signals have less variation, and the output of the filter in

the detected direction is used to separate the Y-signal. As a result, the exact, clear separaation is secured even when the video images are subjected to violent changes. This leads to the production of images free from cross-color or cross-luminance distortion.

Furthermore, the A/D conversion is performed with the sampling pulses having a frequency of four times that of color sub-carrier waves, and a phase in accordance with the axis of the color difference signal, thereby ensuring that reversed sampling points whose color sub-carrier wave phases are reversed to that of a specific sampling point are obtained one line up and below. This means that under this system no two-line memory is required but a single-line memory will suffice, thereby decreasing the production cost.

Referring to Figure 7, a modified version of the embodiment will be described:

There are provided an input terminal 1 for receiving analog composite television signals (composite video signals), a sampling signal generator 3 including a sampling pulse generating circuit (SP) which generates pulses which have a frequency of four times that of color sub-carrier wave, and whose phases are 45° advanced or delayed with relative to the color

signals; and A/D converter 2 which receives the composite television signals P, and converts them into digital signals with using sampling pulses from the sampling signal generator 1; a first delay circuit 43 which delays the input signal by one horizontal scanning period; a second delay circuit 44 which delays the input signal a shorter peiod of time by two sampling periods than one horizontal scanning period; and a third, fourth, fifth, sixth, seventh, and eighth delay circuit 21a, 21b, 21c, 21d, 21e, and 21f each of which delays the input signal by two sampling periods. The 1st to 8th delay circuits constitute a sample signal generator which generates 1st to 8th sample signals as well as the signal to be separated on the basis of the digital signals from the A/D converter 2. The signal to be separated $P(\ell, m)$ is output from the 7th delay circuit 21e. The 1st sample signal $P(\ell-1, m-2)$ is output from the 6th delay circuit 21d, and is a signal delayed a longer period of time by two sampling periods than one horizontal scanning period as compared with the signal to be separated. The 2nd sample signal $P(\ell-1, m)$ is output from the 5th delay circuit 21c, and is a signal delayed one horizontal scanning period as compared with the signal to be separated. The 3rd sample signal $P(\ell-1, m+2)$ is output from the 2nd delay

circuit 44, and is a signal delayed a shorter period of time by two sampling periods than one horizontal scanning period as compared with the signal to be separated. The 4th sample signal $P(\ell, m-2)$ is output from the 8th delay circuit 21f, and is a signal delayed two sampling periods as compared with the signal to be separated. The 5th sample signal $P(\ell, m+2)$ is output from the 1st delay circuit 43, and is a signal advanced two sampling periods as compared with the signal to be separated. The 6th sample signal $P(\ell+1, m-2)$ is output from the 4th delay circuit 21b, and is a signal advanced a shorter period of time by two sampling periods than one horizontal scanning period as compared with the signal to be separated. The 7th sample signal $P(\ell+1, m)$ is output from the 3rd delay circuit 21a, and is a signal advanced one horizontal scanning period as compared with the signal to be separated. The 8th sample signal $P(\ell+1, m+2)$ is output from the A/D converter 2, and is a signal advanced a longer period of time by two sampling periods than one horizontal scanning period as compared with the signal to be separated. There are provided a first addition circuit 22a which adds the 8th sample signal from the A/D converter 2, and the 7th sample signal from the 4th delay circuit 21b; a fourth multiplication circuit 51

which multiplies the signal from the 1st addition circuit 51 1/2 times; a second addition circuit 22b which outputs the sum of the 1st sample signal from the 6th delay circuit 21d and the 3rd smaple signal from the 2nd delay circuit 44; a fifth multiplication circuit 52 which multiplies the signal from the 2nd addition circuit 22b 1/2 times; a second switching circuit 24a which receives the 1/2 sum signal from the 4th multiplication circuit 51 and the 7th sample signal from the 3rd delay circuit 21a, and selectively outputs either of these signals in accordance with a first and second state signal from a switching signal generator 26, that is, upon reception of the 1st state signal the 1/2 sum signal from the 4th multiplication circuit 51 is output, and upon reception of the 2nd state signal the 7th sample signal is output. The reference numeral 24b designates a first switching circuit which receives the 2nd sample signal from the 5th delay circuit 21c and the 1/2 sum signal from the 5th multiplication circuit 51, and selectively outputs either of these signals in accordance with the 1st and 2nd state signal from a switching signal generator 26, that is, upon reception of the 1st state signal the 2nd sample signal is output, and upon reception of the 2nd state signal the 1/2 sum signal is output. There is provided a

second reduction circuit 92 which outputs a difference signal between the selected output from the 1st switching circuit 24b, and that from the 2nd switching circuit 24a. The reference numeral 23a designates a first absolute-value circuit which outputs Tv signal which is an absolute value of the difference signal from the 2nd reduction circuit 92. This absolute-value circuit 23a constitutes a Tv signal generator in combination with the 2nd reduction circuit 92. The reference numeral 94 designates a 4th reduction circuit which outputs a difference signal between the 5th sample signal from the 1st delay circuit 43 and the 4th sample signal from the 8th delay circuit 21e. The reference numeral 23b designates a second absolute-value circuit which outputs the TH signal which is an absolute value of the difference signal from the 4th reduction circuit 94. This circuit 23b constitutes a TH signal generator in combination with the 4th reduction circit 94. The reference numeral 25 designates a comparator which compares the Tv and TH signals from the 1st absolute-value circuit 23a, and the 2nd absolute-value circuit 23b, respectively, and outputs the 1st state signal when Tv is smaller than TH, and the 2nd state signal when TH is smaller than Tv. The Tv signal generator, the TH signal generator,

and the comparator 25 constitute a detecting circuit 80 in combination, for detecting a direction in which the composite television signals have less variation. The reference numeral 22c designates a third addition circuit which outputs the sum of the selected output from the 1st switching circuit 24b, and that from the 2nd switching circuit 24a. The reference numeral 63 designates a first multiplication circuit which multiplies the output from the 3rd addition circuit 22c 1/4 times. The reference numeral 53 designates a third multiplication circuit which multiplies the signal to be separated which is sent from the 7th delay circuit 21e 1/2 times. The reference numeral 93 designates a third reduction circuit which outputs a difference signal between the output from the 3rd multiplication circuit 51 and that from the 1st multiplication circuit 63 as Hc signal, which is a chrominance signal in a horizontal direction. The 3rd addition circuit 22c, the 1st multiplication circuit 63, and the 3rd multiplication circuit 53 constitute a Hc signal generating circuit in combination. The reference numeral 22d designates a fourth addition circuit which outputs the sum of the 5th sample signal from the 1st delay circuit 43 and the 4th sample signal from the 8th delay circuit 21f. The reference numeral 64 designates

a second multiplication circuit which multiplies the output from the 4th addition cirucit 22d 1/4 times. The reference numeral 95 designates a fifth reduction circuit wich outputs a difference signal between the output signal from the 3rd multiplication circuit 51 and that from the 2nd multiplication circuit 64 as Vc signal, which is a chrominance signal in a vertical direction. The 4th addition circuit 22d and the 2nd multiplication circuit 64 constitute the Vc signal generating circuit. The sample signal generating circuit, the Hc signal generating circuit, and the Vc signal generating circuit constitute a vertical filter and a horizontal filter 70. The reference numeral 24c designates a selecting circuit which, receiving the Hc signal from the 3rd reduction circuit 93 as well as the Hv signal from the 5th reduction circuit 95, and also receiving the 1st and 2nd state signals from the comparator 25, selectively outputs the Hc signal to the chrominance signal output terminal 10 as a chrominance signal upon reception of the 1st state signal, and selectively outputs the Vc signal to the same terminal 10 as a chrominance signal upon reception of the 2nd state signal. The reference numeral 91 designates a first reduction circuit which outputs a difference signal between the signal to be separated from the 5th

delay circuit 21, and the chrominance signal of the selected output from the selecting circuit 24c to a luminance signal terminal 11 as a luminance signal.

The circuit shown in Figure 7 is operated as follows:

The sampling signal generating circuit 3 is an oscillating circuit which synchronously oscillates at a frequency fs which is four times the frequency fsc of the color sub-carrier wave of the composite television signal which is applied to the input terminal 1, the sampling pulse having a phase which is 45° advanced or delayed with relative to the axis of the color difference signals (R-Y) and (B-Y). The sampling signal output from the circuit 3 is applied to the A/D converter 2, which then converts the analog composite signals received at the input terminal 1 into digital signals. In this way the composite color T.V. signals of PAL system are converted into sample signal series, which will appear on the screen as shown in Figure 8 when the phase of C-signals is noted.

Referring to Figures 9 and 10, the embodiment shown in Figure 7 will be described in greater detail, wherein the picture in Figure 9 has the addition of reference numerals and characters to that in Figure 8. The situatin in Figure 9 will be described by using the

circuit in Figure 7:

Now, suppose that the A/D converter 2 outputs a sample value at the point P9 as the 8th sample signal at a time T. Then the 3rd delay circuit 21a outputs a sample value at the point P8 as the 7th sample signal; the 4th delay circuit 21b outputs a sample value at the point P7 as the 6th sample signal; the 1st delay circuit 43 outputs a sample value at the point P6 as the 4th sample signal; the 7th delay circuit 21e outputs a sample value at the point P5 as a signal to be separated; the 8th delay circuit 21f outputs a sample value at the point P4 as the 4th sample signal; the 2nd delay circuit 44 outputs a sample value at the point P3 as the 3rd sample signal; the 5th delay circuit 21c outputs a sample value at the point P2 as the 2nd sample signal, and the 6th delay circuit 21d outputs a sample value at the point P1 as the 1st sample signal. In this case the point 5 is the point of the signal which is to be separated into Y and C signals.

In the case of Figure 9 the switching signal generating circuit 26 outputs a control signal of the 1st state signal to the 2nd switching circuit 24a in such a manner as to allow the output signal of the 1st 1/2 times circuit 51 to pass, and also outputs a

control signal of the 1st state signal to the 1st switching circuit 24b in such a manner as to allow the output signal of the 5th delay circuit 21c to pass.

The 1st addition circuit 22a adds the output of the A/D converter 2 and that of the 4th delay circuit 21b, and the 4th multiplication circuit 51 multiplies the output of the 1st addition circuit 22a 1/2 times. As a result, the output of the 1st addition circuit 22a, that is, the output of the 2nd switching circuit 24a is expressed by:

$$1/2\ ([\text{the sample value at the point P9}] + [\text{the sample value at the point P7}])$$

The output of the 1st switching circuit 24b provides a sample value at the point P2.

The 3rd addition circuit 22c adds the output of the 2nd switching circuit 24a and that of the 1st switching circuit 24b, and the 1st multiplication circuit 63 multiplies the output of the addition circuit 22c 1/4 times. The 3rd multiplication circuit 53 multiplies the output of the 7th delay circuit 21e 1/2 times. The 3rd reduction circuit 93 reduces the output of the 1st multiplication circuit 63 from the output of the 3rd multiplication circuit 53. Consequently, the output signal Hc of the 1st reduction circuit 93 is expressed by:

- 1 / 4 (1/2 [the sample value at the point P9])
+ [the sample value at the point P7])
+ 1 / 2 (the sample value at the point P5)
- 1 / 4 (the sample value at the point P2)

The 4th addition circuit 22d adds the output of the 1st delay circuit 43 and that of the 8th delay circuit 21f, and the 2nd multiplication circuit 64 multiplies the output of the addition circuit 22d 1/4 times. The 5th reduction circuit 95 reduces the output of the 2nd multiplication circuit 64 from that of the 3rd multiplication circuit 53, the output signal of the reduction circuit 95 Vc is expressed by:

- 1 / 4 (the sample value at the point P4)
+ 1 / 2 (the sample value at the point P5)
- 1 / 4 (the sample value at the point P6)

The output signals of the 2nd switching circuit 24a, and the 1st switching circuit 24b are applied to the 2nd reduction circuit 92, the output of which is taken an absolute value by the 1st absolute-value circuit 23a. The output signal Tv of the 1st absolute-value circuit 23a is expressed by:

Tv = | 1 / 2 ([the sample value at the point P9]
+ [the sample value at the point P7])
- (the sample value at the point P2) |

The outputs of the 1st delay circuit 43 and the

8th delay circuit 21f are applied to the 4th reduction circuit 94, the output of which is taken an absolute value by the 2nd absolute-value circuit 23b. The output signal TH of the 2nd absolute-value circuit 23b is expressed by:

$$TH = |(\text{the sample value at the point P4}) - (\text{the sample value at the point P6})|$$

The output signal Tv of the 1st absolute-value circuit 23a, and the output signal TH of the 2nd absolute-value circuit 23b are applied to the comparator 25, which compares the Tv and TH, and sends the 1st or 2nd state signal as a control signal to the selecting circuit 24c. At this stage the selecting circuit 24c has received the output signals of the 3rd reduction circuit 93 and the 5th reduction circuit 95. When Tv is smaller than TH, the comparator 25 outputs the 1st state signal to the switching circuit 25c so that the output thereof be that of the 3rd reduction circuit 93. When Tv is equal to, or larger than TH, the comparator 25 outputs the 2nd state signal to the switching circuit 24c so that the output thereof be the output of the 5th reduction circuit 95.

Under the illustrated system the adjacent picture element signals whose color sub-carrier wave phases are reversed with relative to the particular picture

element are used to detect a direction in which the signals have little variation, and the picture elements in the detected direction are used to separate the C signals from the composite television signals. Thus the system ensures the exact, clear separation.

The example of Figure 10 will be described with reference to Figure 7:

Now suppose that the A/D converter 2 outputs a sample value at the point P9 (the 8th sample signal) at a time T. Then the 3rd delay circuit 21a outputs a sample value at the point P8 as the 7th sample signal; the 4th delay circuit 21b outputs a sample value at the point P7 as the 6th sample signal; the 1st delay circuit 43 outputs a sample value at the point P6 as the 5th sample signal; the 7th delay circuit 21c outputs a sample value at the point P5 as the signal to be separated; the 8th delay circuit 21f outputs a sample value at the point P4 as the 4th sample signal; the 2nd delay circuit 44 outputs a sample value at the point P3 as the 3rd sample signal; the 5th delay circuit 21e outputs a sample value at the point P2 as the 2nd sample signal; and the 6th delay circuit 21d outputs a sample value at the point P1 as the 1st sample signal.

In the case of Figure 10 the switching signal

generating circuit 26 outputs a control signal to the 2nd switching circuit 24a so as to allow the output signal of the 3rd delay circuit 21a to pass, and outputs a control signal to the 1st switching circuit 24b so as to allow the output signal of the 5th multiplication circuit 52 to pass.

The 2nd addition circuit 22b adds the output of the 2nd delay circuit 44 and that of the 6th delay circuit 21d, and the 5th multiplication circuit 52 multiplies the output of the 2nd addition circuit 22b 1/2 times. Therefore, the output of the 2nd addition circuit 22b, that is, the output signal of the 1st switching circuit 24b is expressed by:

1 / 2 (the sample value at the point P3)
+ (the sample value at the point P1)

The output signal of the 2nd switching circuit 24a becomes the sample value at the point P8.

The 3rd addition circuit 22c adds the output of the 2nd switching circuit 24a and the 1st switching circuit 24b, and the 1st multiplication circuit 63 multiplies the output of the addition circuit 22c 1/4 times. The 3rd multiplication circuit 53 multiplies the output of the 7th delay circuit 21e 1/2 times. The 3rd reduction circuit 93 reduces the output of the 1st multiplication circuit 63 from the output of the 3rd

multiplication cirucit 53. Thus the output signal Hc of the reduction circuit 93 is expressed by:

$$-1/4\,(1/2\,[\text{the sample value at the point P3}] + [\text{the sample value at the point P1}]) + 1/2\,(\text{the sample value at the point P5}) - 1/4\,(\text{the sample value at the point P8})$$

The 1st addition circuit 22d adds the output of the 1st delay circuit 43 and that of the 8th delay circuit 21f, and the 2nd multiplication circuit 64 multiplies the output of the addition circuit 22d 1/4 times. The 5th reduction circuit 95 reduces the output of the 2nd multiplication circuit 64 from the output of the 3rd multiplication circuit 53. The output signal Vc of the reduction circuit 95 is expressed by:

$$-1/4\,(\text{the sample value at the point P4}) + 1/2\,(\text{the sample value at the point P5}) - 1/4\,(\text{the sample value at the point P6})$$

The outputs of the 2nd switching circuit 24a and the 1st switching circuit 24b are applied to the 2nd reduction circuit 92, the output of which is taken an absolute value by the 1st absolute-value circuit 23a. As a result the output signal Tv of the 1st absolute-value circuit 23a is expressed by:

$$Tv = |1/2\,(\text{the sample value at the point P3}) + (\text{the sample value at the point P1})$$

- (the sample value at the point P8)|

The outputs of the 1st delay circuit 43 and the 8th delay circuit 21f are applied to the 4th reduction circuit 94, the output of which is taken an absolute value by the 2nd absolute-value circuit 23b. As a result the output signal TH of the 2nd absolute-value circuit 23b is expressed by:

TH = |(the sample value at the point P4)
- (the sample value at the point P6)|

The output signal Tv of the 1st absolute-value circuit 23a and the output signal TH of the 2nd absolute-value circuit 23b are applied to the comparator 25, which compares these signals Tv and TH thereby to send the 1st or 2nd state signal as a control signal to the switching cirucit 24c. The switching circuit 24c has already received the output signals of the 3rd reduction circuit 93 and the 5th reduction circuit 95. As a result, when Tv is smaller than TH, the comparator 25 outputs the 2nd state signal as a control signal to the switching circuit 24c so that the output thereof be the output of the 3rd reduction circuit 93. When Tv is equal to, or larger than TH, the comparator 25 outputs the 2nd state signal as a control signal to the switching circuit 24c so that the output thereof be the output of the 5th

reduction circuit 95.

Under the illustrated system the adjacent picture element signals whose color sub-carrier wave phases are reversed with relative to that of the particular picture element are used to detect a direction in which the signals have less variation, and the picture elements in the detected direction are used to separate the C signals from the composite television signals. Thus the system ensures an exact, clear separation of C and Y signals.

The operation of the switching signal generating circuit 26 will be described:

As evident from Figure 7, when a particular sampling point is noted, there are two cases in which sampling points whose color sub-carrier wave phases are reversed to that of the particular sampling point are found one line up and below. Figure 9 illustrates the case in which the sampling points whose color sub-carrier wave phases are reversed to that of the noted point P5 are found one line up. Figure 10 illustrates the other case, that is, they are found one line below. To embody a Y- and C-signal separating filter, it is required for the switching pulse generating cirucit 26 to generate control pulses whereby the 2nd switching circuit 24a and the 1st

switching circuit 25b are switched depednding on the respective cases of Figures 9 and 10, at each of the noted sampling point. Now, suppose that the point P5 is a point where the intended separation is to be performed. The sampling values at this point P5 and a corresponding point P2 one line up are compared, and an absolute value of the resulting difference is taken. In addition, the sampling values at the point P5 and a corresponding point P8 one line below are compared, and an absolute value of the resulting difference is taken. These absolute values are compared:

$$\left|\text{(the sample value at the point P5)} - \text{(the sample value at the point P2)}\right| > \left|\text{(the sample value at the point P5)} - \text{(the sample point at the point P8)}\right|$$

If the above relationship is established, the switching signal generating circuit 26 outputs a control signal in such a manner as to allow the 2nd switching circuit 24a to pass the output signal of the 4th multiplication circuit 51, and to allow the 1st switching circuit 24b to pass the output signal of the 5th delay circuit 21c.

In the opposite case (Figure 10) the switching signal generating circuit 26 outputs a control signal so as to allow the 2nd switching circuit 24a to pass

the output signal of the 3rd delay circuit 21a, and to allow the 1st switching circuit 24b to pass the output signal of the 5th multiplication circuit 52.

When the phase of the sampling signal is fixed, the patterns shown in Figure 8 are equally fixed. Therefore, it is possible to construct the switching signal generating circuit 26 so that the 2nd and 1st switching circuits 24a, 24b can be switched at each sampling point on one line through the recognition of the horizontal line of the input signal.

The 1st reduction circuit (luminance signal output circuit) 91 reduces the output of the selecting circuit 24c from that of the 7th delay circuit 21e. The output signal of the 7th delay circuit 21e is a composite television signal, and the output signal of the selecting circuit 24c is a C signal which has been separated from the composite television signal. As a result, the output signal of the 1st multiplication circuit 91 becomes a Y signal.

As evident from the foregoing description, the sampling points one line up and below or the sampling points two points forward and backward on the same line are used to perform the separation of Y- and C-signals. An advantage of this system is that each sampling point has little variation, which results in the exact

separation of Y- and C-signals. Furthermore, the adjacent samling points are used to detect a direction in which the signals have less variation, and the output of the filter in the detected direction is used to separate the Y signals. This method ensures the exact and clear separtion regardless of the situation in which video images are subjected to violent changes, and that the images free from cross-color or cross-luminance distortion is reproduced.

In the embodiment illustrated in Figure 7, the A/D conversion is performed with the use of a sampling pulse having a frequency of four times that of the color sub-carrier wave, and whose phase is 45 advanced or delayed with relative to the color difference signal. This makes it possible to obtain a reversed sampling point whose color sub-carrier wave phase is reversed with relative to that of the desired sampling point one line up and below thereof, thereby eliminating the necessity of using a two-line memory. The use of a single-line memory leads to the decreased production cost.

CLAIMS:

1. A filter for separating luminance and chrominance signals from the composite television signals of PAL system, comprising:

a sampling signal generator for generating a sampling signal having a frequency of four times that of color sub-carrier wave, and whose phase is in accordance with the U and V axis of the chrominance signal;

an A/D converter for converting the input analog composite television signals into digital signals with the use of the sampling signal;

a vertical and a horizontal filter for separating a chrominance signal at each particular sampling point, with the use of sample value obtained at each sampling point through the A/D conversion, the sample values of first adjacent sampling points adjacent to each particular point, wherein the first adjacent points have a reversed color sub-carrier wave phase to that of each particular point, and wherein the first adjacent point are one line up or below of each particular point, or of second adjacent

points on the same line as that of each particular point, wherein the second adjacent points have a reversed color sub-carrier wave phase to that of each particular point;

a detecting means for detecting a direction in which the signal has less variation, with the use of the sample values of the first and second adjacent sampling points;

a selecting means for selecting either output of the vertical or horizontal filter in the direction detected by the detecting means; and

a luminance signal generator for outputting luminance signals by separating chrominance signals from the digitized composite television signals.

2. A separating filter as defined in Claim 1, wherein as the first adjacent sampling points those which are selected on the basis of the value of the particular point, and that of the sampling point one line up or below are used.

3. A separating filter as defined in Claim 1, wherein as the second adjacent sampling points those which are selected by switching the sampling points

having a predetermined positional relation with the particular point at each particular point in the order determined by the line of the input PAL signals.

4. A filter for separating luminance and chrominance signals, comprising:

a sampling signal generator for generating sampling signals having a frequency of four times that of color sub-carrier wave, and whose phase is in accordance with the U- and V-axis of the chrominance signal;

an A/D converter for converting the input analog composite television signals having luminance and chrominance signals into digital signals with the use of the sampling signals;

a sample signal generator for outputting, a signal to be separated, a first sample signal delayed a longer period of time by one sampling period than one horizontal scanning period as compared with the signal to be separated, a second sample signal delayed a shorter period of time by one sampling period than one horizontal scanning period as compared with the signal to be separated, a third sample signal delayed two

sampling periods as compared with the signal to be separated, a fourth sample signal advanced two sampling periods as compared with the signal to be separated, a fifth sample signal advanced a shorter period of time by one sampling period than one horizontal scanning period as compared with the signal to be separated, and a sixth sample signal advanced a longer period of time by one sampling period than one horizontal scanning period as compared with the signal to be separated;

a switching signal generator for outputting a first and a seocnd state signal;

a first switching means for receiving the first and second sample signal from the sample signal generator, and selectively outputting either of these sample signals in accordance with the first state signal or the second state signal;

a second switching means for receiving the fifth and sixth sample signals from the sample signal generator, and selectively outputting either of these sample signals in response to the first state signal or the

second state signal;

a Tv signal outputting means for receiving the sample signal selected by the first switching means, and the sample signal selected by the second switching means, and outputting a Tv signal which is a high-frequency component of the luminance signal in the vertical direction;

a TH signal outputting means for receiving the third and fourth sample signals from the sample signal generator, and outputting a TH signal which is a high-frequency component of the luminance signal in the horizontal direction;

a comparator for comparing the Tv and TH signals, and outputting the first state signal when the Tv signal is smaller than the TH signal,and the second state signal when TH signal is smaller than the Tv signal;

a Hc signal generator for outputting a chrominance signal Hc in a horizontal direction on the basis of the signal to be separated from the sample signal generator, a sample signal selected by the first

switching means, and a sample signal selected by the second switching means;

a Vc signal generator for outputting a chrominance signal Vc in a vertical directin on the basis of the signal to be separated and the third and fourth sample signal from the sample signal generator;

a selecting means for receiving the chrominance signals Hc and Vc, and the first and second state signals from the comparator, and outputting the chrominance signal Hc as a chrominance signal when the first state signal is input, and the chrominance signal Vc as a chrominance signal when the second state signal is input; and

a luminance signal generator for outputting a luminance signal on the basis of the chrominance signal from the selecting means, and the signal to be separated from the sample signal generator.

5. A separating filter as defined in Claim 4, wherein the first switching means outputs the second sample signal in response to the first state signal from the switching signal gnerator whereas it outputs

the first sample signal in response to the second state signal, and wherein the second switching means outputs the fifth sample signal in response to the first state signal from the switching signal generator whereas it outputs the sixth sample signal in response to the second state signal.

6. A separating filter as defined in Claim 5, wherein the switching signal generator outputs the first state signal when the absolute value of the difference between the sample value of the signal to be separated from the sample signal generator and that of the first sample signal is smaller than the absolute value of the difference between the sample value of the signal to be separated and that of the second sample signal, whereas it outputs the second state signal when the absolute value of the difference between the signal to be separated and that of the second sample signal smaller than the absolute value of the difference between the sample value of the signal to be separated and that of the first sample signal.

7. A separating filter as defined in Claim 5, wherein the switching signal generator has a frequency of four times that of the color sub-carrier wave, and outputs the first state signal and the second state signal, alternately.

8. A separating filter as defined in Claim 4, wherein the sample signal generator comprises a first delay means for outputting the digital signal from the A/D converter as a sixth sample signal, and a fourth sample signal by delaying the sixth sample signal a shorter period of time by one sampling period than one horizontal scanning period; a fifth delay means for outputting the signal to be separated by delaying the fourth sample signal from the first delay means by two sampling periods; a second delay means for outputting a second sample signal by delaying the signal to be separated from the fifth delay means a shorter period of time by one sampling period than one horizontal scanning period; a fourth delay means for outputting a first sample signal by delaying the second sample signal from the second delay means by two sampling periods; a sixth delay means for outputting a third sample signal by delaying the signal to be separated from the fifth delay means by two sampling periods; and a third delay means for outputting a fifth sample signal by delaying the sixth sample signal by two sampling periods.

9. A separating filter as defined in Claim 4, wherein the Hc signal generator comprises a first addition means for outputting the sum of the selected

output of the first or second sample signal from the first switching means, and the selected output of the fifth or sixth sample signal from the second switching means; a first multiplication means for multiplying the signal from the first addition means 1/4 times; a third multiplication means for multiplying the signal to be separated from the sample signal generator 1/2 times; a third reduction means for outputting as the Hc signal the difference signal between the signal from the third multiplication means and the signal from the first multiplication means, and wherein the Vc signal generator comprises a second addition means for outputting the sum of the third and fourth sample signals from the sample signal generator; a second multiplication means for multiplying the signal from the second addition means 1/4 times; and a second reduction means for outputting as the Vc signal the difference signal between the signal from the third multiplicaton means and the signal from the second multiplication means.

10. A separating filter as defined in Claim 4, wherein the Tv signal generator comprises a second reduction means for outputting the difference signal between the selected output of the first or second sample signal from the first switching means and the

selected output of the fifth or sixth sample signal from the second switching means, and a first absolute value means for outputting the absolute value of the signal from the second reduction means as a Tv signal, and wherein the TH signal generator comprises a fourth reduction means for outputting the difference signal between the third sample signal and the fourth sample signal from the sample signal generator, and a second absolute-value means for outputting the absolute value of the signal from the fourth reduction means as the TH signal.

11. A filter for separating luminance and chrominance signals from the composite television signals of PAL system, comprising:

a sampling signal generator for generating a sampling signal having a frequency of four times that of the color sub-carrier wave, and whose phase is 45° advanced or delayed with relative to the color difference signal;

an A/D converter for converting the input analog composite television signals into digital signals with the use of the sampling signals;

a vertical filter and a horizontal filter for

separating chrominance signals at each particular sampling point, with the use of a sample value obtained at each sampling point through the A/D conversion, the sample values of first adjacent sampling points adjacent to each particular point, wherein the first adjacent sampling points have a reversed color sub-carrier wave phase to that of each particular point, and wherein the first adjacent points are one line up or below of each particular point, or second adjacent points on the same line as that of each particular point, wherein the second adjacent points have a reversed color sub-carrier wave phase to that of each particular point;

a detecting means for detecting a direction in which the signal has less variation, with the use of the sample values of the first and second adjacent sampling points;

a selecting means for selecting either of the outputs of the vertical filter and the horizontal filter in the direction detected by the detecting means; and

a luminance signal generator for outputting

the luminance signal by removing the chrominance signal which is the output from the selecting means from the composite television signal.

12. A separating filter as defined in Claim 11, wherein as the first adjacent sampling points those which are selected in accordance with the value of the particular point, and that of the samling point one line up or below are used.

13. A separating filter as defined in Claim 11, wherein as the second adjacent sampling points those which are selected by switching the sampling points having a predetermined positional relation with the particular point at each particular point in the order determined by the line of the input PAL signals.

14. A filter for separating luminance and chrominance signals from the composite television signals of PAL system, comprising:

a sampling signal generator for generating a sampling signal having a frequency of four times that of the color sub-carrier wave, and whose phase is 45 advanced or delayed with relative to the chrominance signal;

an A/D converter for converting the input composite television signals including the

luminance and chrominance signals into digital signals with the use of the sampling signals from the sampling signal generator;

a sample signal generator for outputting upon reception of the digital signals from the A/D converter, a signal to be separated, a first sample signal delayed a longer period of time by two sampling periods than one horizontal scanning period as compared with the signal to be separated, a second sample signal delayed one horizontal scanning period as compared with the signal to be separated, a third sample signal delayed a shorter period of time by two sampling periods than one horizontal scanning period as compared with the signal to be separated, a fourth sample signal delayed two sampling periods as compared with the signal to be separated, a fifth sample signal advanced two sampling periods as compared with the signal to be separated, a sixth sample signal advanced a shorter period of time by two sampling periods than one horizontal scanning period as compared

with the signal to be separated; a seventh sample signal advanced by one horizontal scanning period as compared with the signal to be separated, and an eighth sample signal advanced a longer period of time by two sampling periods than one horizontal scanning period as compared with the signal to be separated;

a switching signal generator for outputting the first and second state signal;

a first switching means for receiving a first 1/2 sum sample signal obtained by multiplying the sum of the first and third sample signal 1/2 times and a second sample signal from the sample signal generator, and selectively outputting the first 1/2 sum sample signal or the second sample signal;

a second switching means for receiving a second 1/2 sum sample signal obtained by multiplying the sum of the sixth and eighth sample signal 1/2 times and a seventh sample signal from the sample signal generator, and selectively outputting the second 1/2 sum sample signal or the seventh

sample signal;

a Tv signal generator for receiving the sample signal selectively output from the first switching means, and the sample signal selectively output from the second switching means, and outputting a high-frequency component of the luminance signal in a vertical direction as a Tv signal;

a TH signal generator for receiving the fourth and fifth sample signal from the sample signal generator, and outputting a high-frequency component of the luminance signal in a horizontal direction as a TH signal;

a comparator for comparing the Tv and TH signals from the Tv and TH signal generators, and outputting the first state signal when the Tv signal is smaller than the TH signal, and the second state signal when the TH signal is smaller than the Tv signal;

a Hc signal generator for outputting chrominance signal Hc in a horizontal direction on the basis of the signal to be

separated from the sample signal generator, and the sample signal selectively output from the first switching means, and the sample signal selectively output from the second switching means;

a Vc signal generator for outputting chrominance signals in a vertical direction on the basis of the signal to be separated, and the fourth and fifth sample signal from the sample signal generator;

a selecting means for receiving the chrominance signals Hc and Vc from the Hc signal generator and the Vc signal generator, and the first and second state signal from the comparator, and outputting the chrominance signal Hc as a chrominance signal when the first state signal is received, and the chrominance signal Vc as a chrominance signal when the second state signal is received; and

a luminance signal generator for outputting luminance signals on the basis of the chrominance signals from the selecting means, and the signal to be separated from

the sample signal generator.

15. A separating filter as defined in Claim 14, wherein the first switching means selectively outputs the third sample signal in response to the first state signal from the switching signal generator, and a first 1/2 sum sample signal in response to the second state signal, and wherein the second switching means outputs a second 1/2 sum sample signal in responce to the first state signal, and the seventh sample signal in response to the second state signal.

16. A separating filter as defined in Claim 15, wherein the switching signal generator outputs the first state signal when the absolute value of the difference between the sample value of the signal to be separated and that of the second sample signal from the sample signal generator is smaller than the absolute value of the difference between the sample value of the signal to be separated and that of the seventh sample signal, and outputs the second state signal when the absolute value of the difference between the sample value of the signal to be separated and that of the seventh sample signal is smaller than the absolute value of the difference between the sample value of the signal to be separated and that of the second sample signal.

17. A separating filter as defined in Claim 15, wherein switching signal generator outputs the first and second state signal, alternately, at a frequency of four times that of the color sub-carrier wave.

18. A separating filter as defined in Claim 14, wherein the sample signal generator comprises a first delay means for outputting the digital signals from the A/D converter as an eighth sample signal, and a fifth sample signal by delaying the eighth sample signal one horizontal scanning period; a seventh delay means for outputting the signal to be separated by delaying the fifth sample signal from the first delay means by two sampling periods; a second delay means for outputting a third sample signal by delaying the signal to be separated from the seventh delay means a shorter period of time by two sampling periods than one horizontal scanning period; a fifth delay means for outputting a second sample signal by delaying the third sample signal from the second delay means by two sampling periods; a sixth delay means for outputting a first sample signal by delaying the second sample signal from the fifth delay means by two sampling periods; an eighth delay means for outputting a fourth sample signal by delaying the signal to be separated from the seventh delay means by two sampling periods; a third

delay means for outputting a seventh sample signal by delaying the eighth sample signal by two sampling periods, and a fourth delay means for outputting an eighth sample signal by delaying the seventh sample signal from the third delay means by two sampling periods.

19. A separating filter as defined in Claim 14, wherein the Hc signal generator comprises a third addition means for outputting the sum of the selected output of the second sample signal or the first 1/2 sum sample signal from the first switching means, and the selected output of the second 1/2 sum sample signal or the seventh sample signal from the second switching means; a first multiplication means for multiplying the sum signal from the third addition means 1/4 times; a third multiplicaton means for multiplying the signal to be separated from the sample signal generator 1/2 times; a third reduction means for outputting as a Hc signal the difference between the multiplied signal from the third multiplication means and the multiplied signal from the first multiplication means, and wherein the Hc signal generator comprises a fourth addition means for outputting the sum of the fourth and fifth sample signals from the sample signal generator; a second multiplication means for multiplying the sum

signal from the fourth addition means 1/4 times, and a second reduction means for outputting as a Vc signal the difference between the multiplied signal from the third multiplication means and the multiplied signal from the second multiplication means.

20. A separating filter as defined in Claim 14, wherein the Tv signal generator comprises a second reduction means for outputting the difference between the selected output of the second sample signal or the first 1/2 sum sample signal from the first switching means and the selected output of the second 1/2 sum sample signal or the seventh sample signal from the second switching means, and a first absolute-value means for outputting as a Tv signal the absolute-value of the difference signal from the second reduction means, and wherein the TH signal generator comprises a fourth reduction means for outputting the difference signal between the fourth sample signal and the fifth sample signal from the sample signal generator, and a second absolute-value means for outputting as a TH signal the absolute value of the difference signal from the fourth reduction means.

FIG.2.(PRIOR ART)

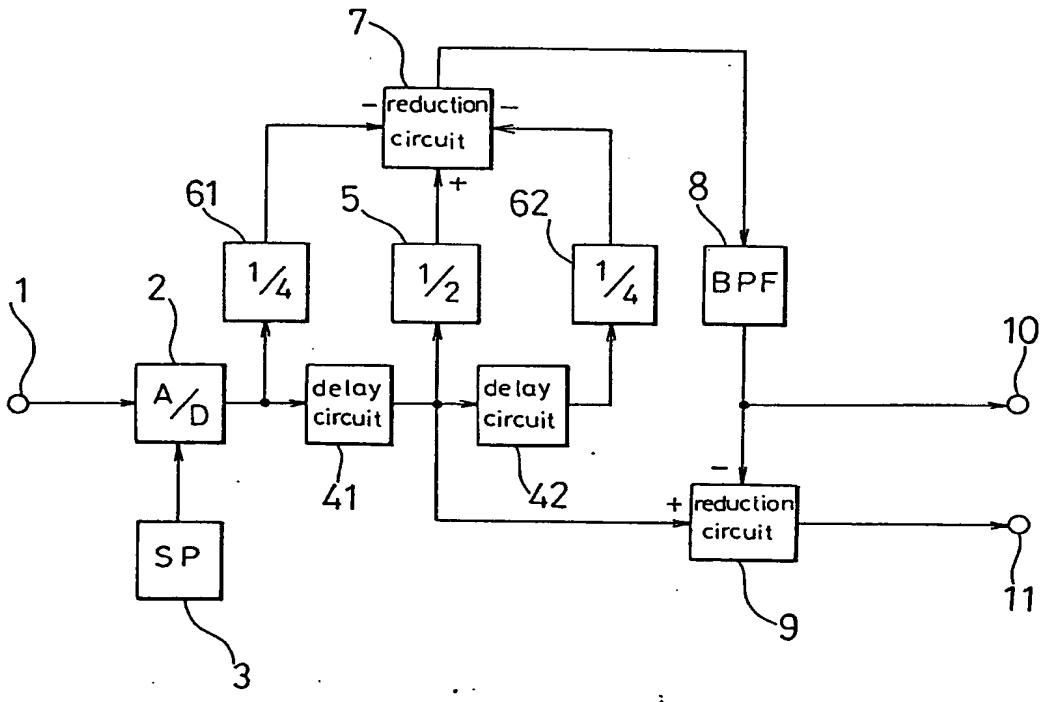

FIG 1. (PRIOR ART)

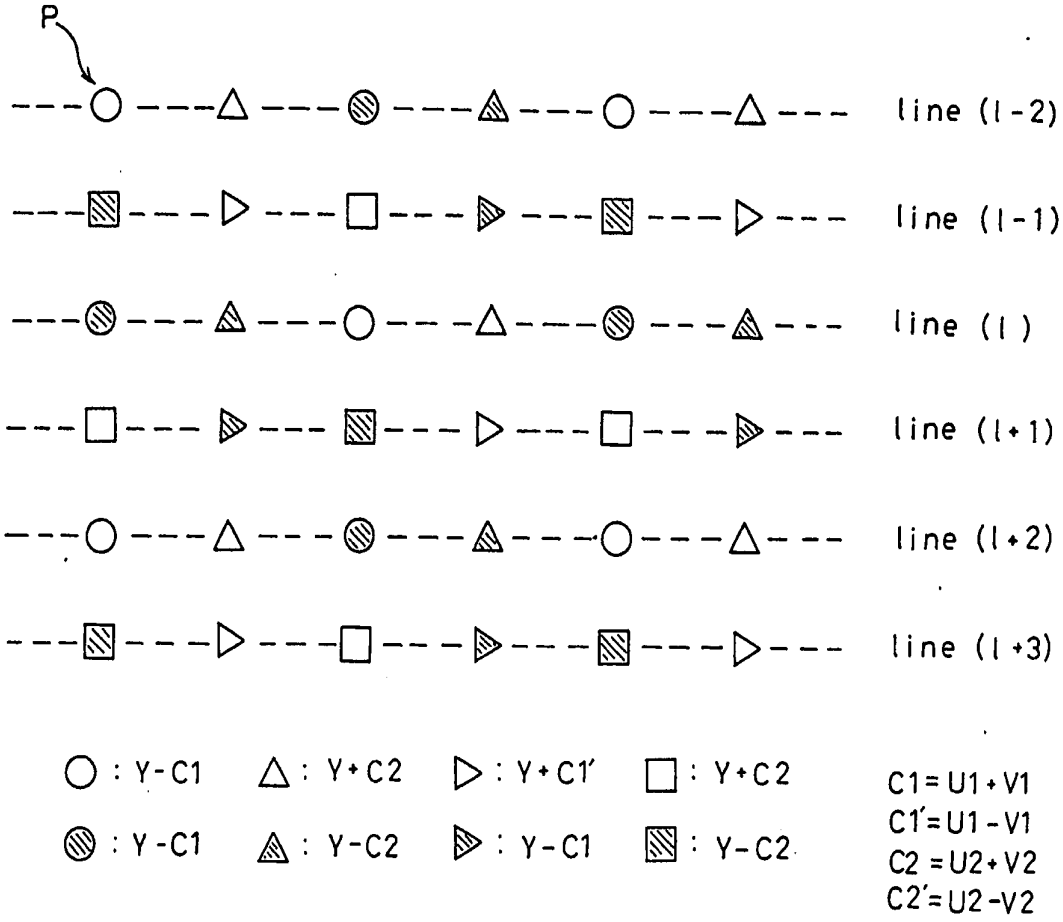




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FIG.3.

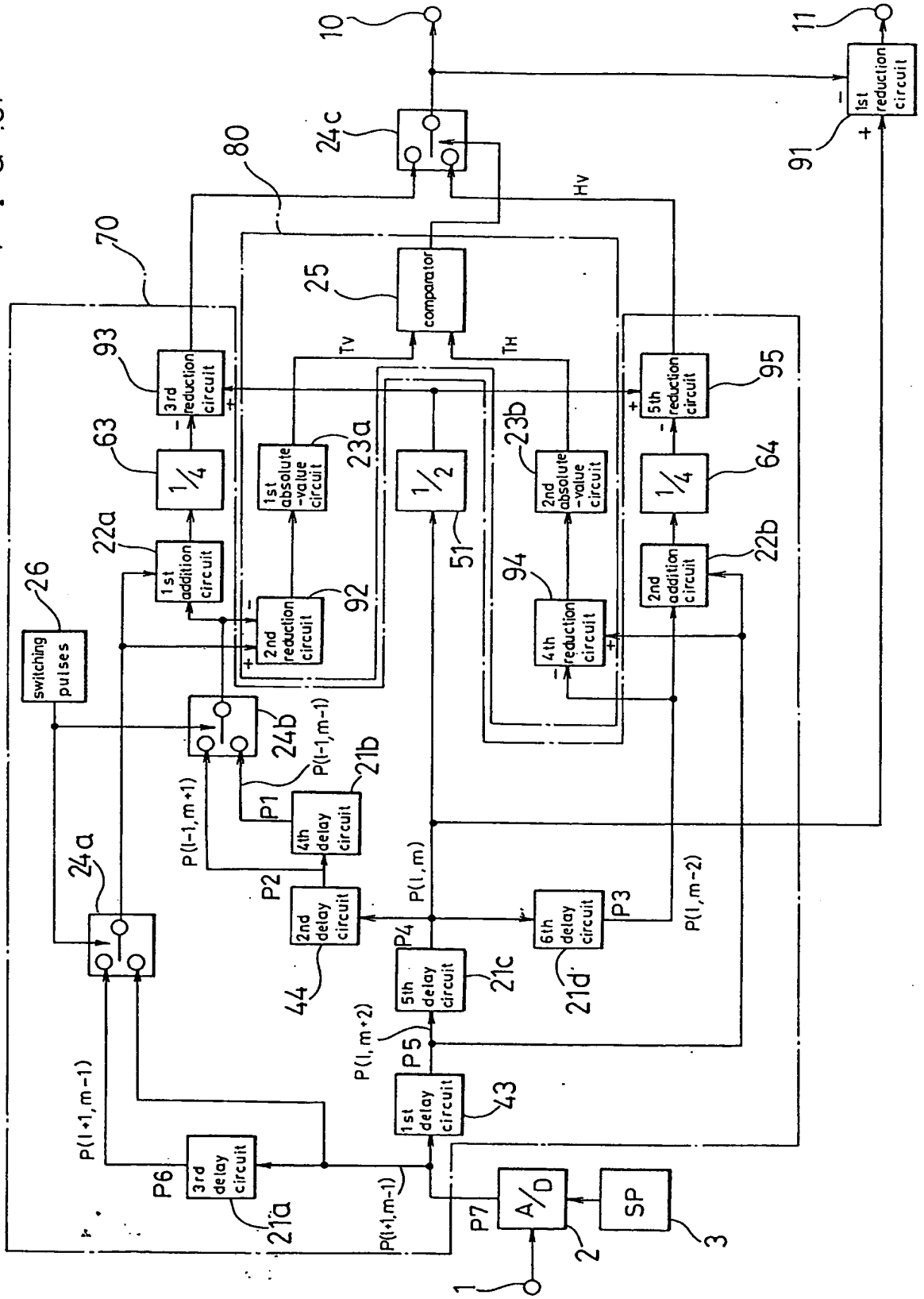
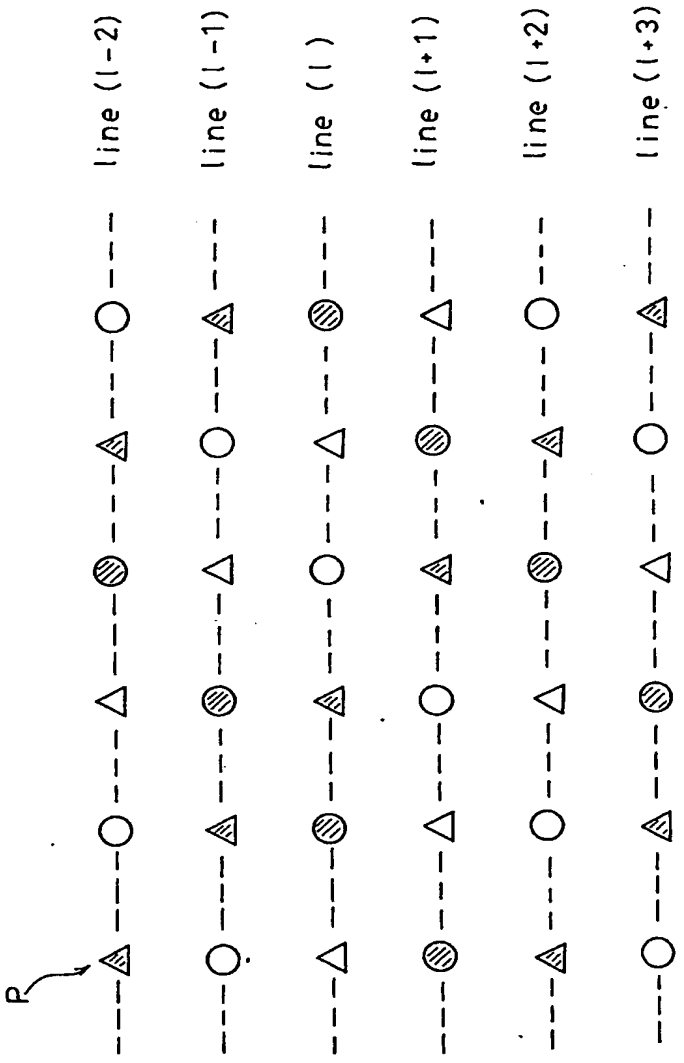

10
11
80
24c
Hv
70
25
comparator
Tv
TH
93
3rd reduction circuit
63
1/4
1st absolute -value circuit
23a
1/2
23b
2nd absolute -value circuit
1/4
64
5th reduction circuit
95
22a
1st addition circuit
2nd reduction circuit
92
51
94
4th reduction circuit
2nd addition circuit
22b
26
switching pulses
24b
P(l-1,m-1)
21b
P(l-1,m+1)
P1
4th delay circuit
24a
P2
2nd delay circuit
P(l,m)
6th delay circuit
P3
P(l,m-2)
44
P4
5th delay circuit
21c
21d
P(l,m+2)
P5
1st delay circuit
43
P(l+1,m-1)
3rd delay circuit
P6
21a
P(l+1,m-1)
P7
A/D
SP
2
3
1
91
1st reduction circuit

FIG 4.



F I G .5.

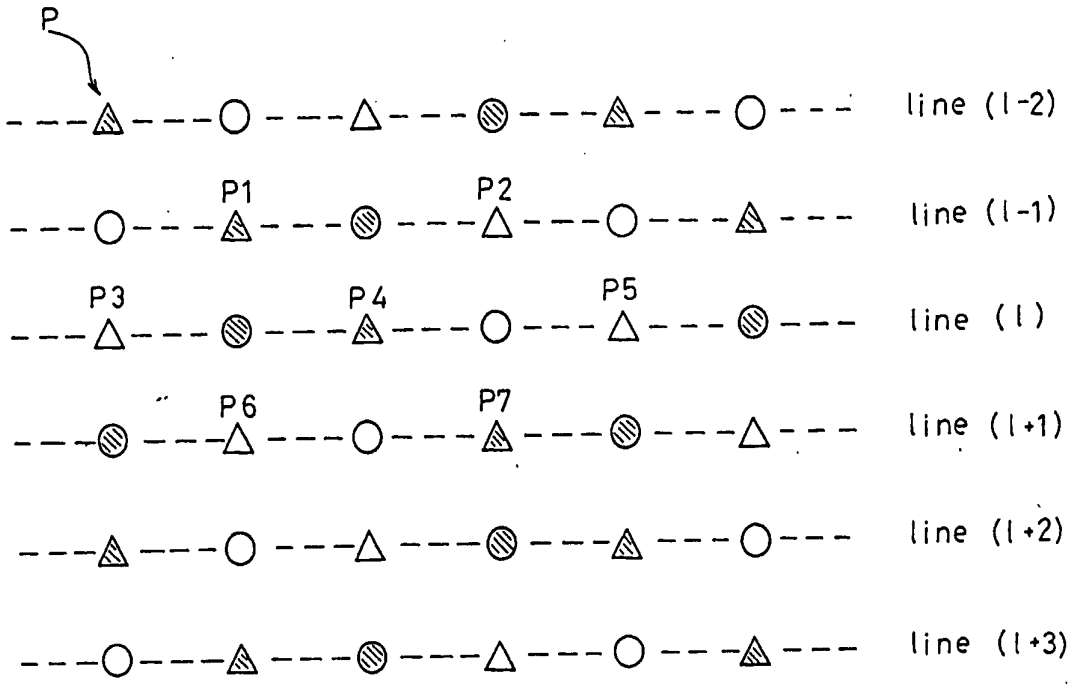





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FIG.6.

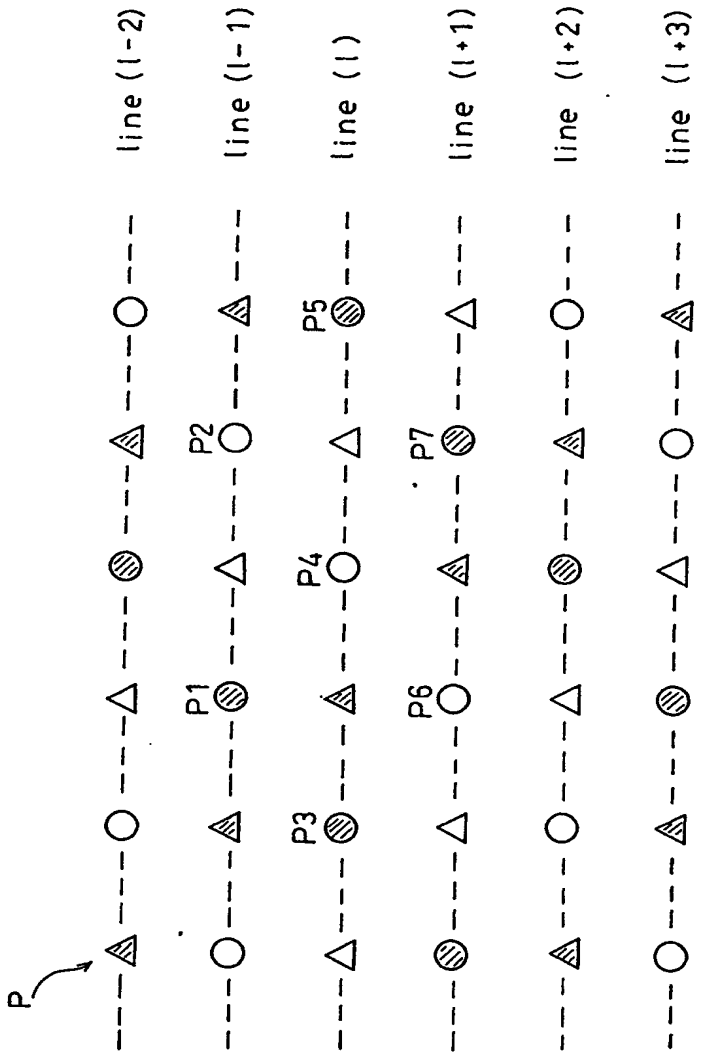

P
P1
P2
P3
P4
P5
P6
P7
line (l-2)
line (l-1)
line (l)
line (l+1)
line (l+2)
line (l+3)

FIG. 7.

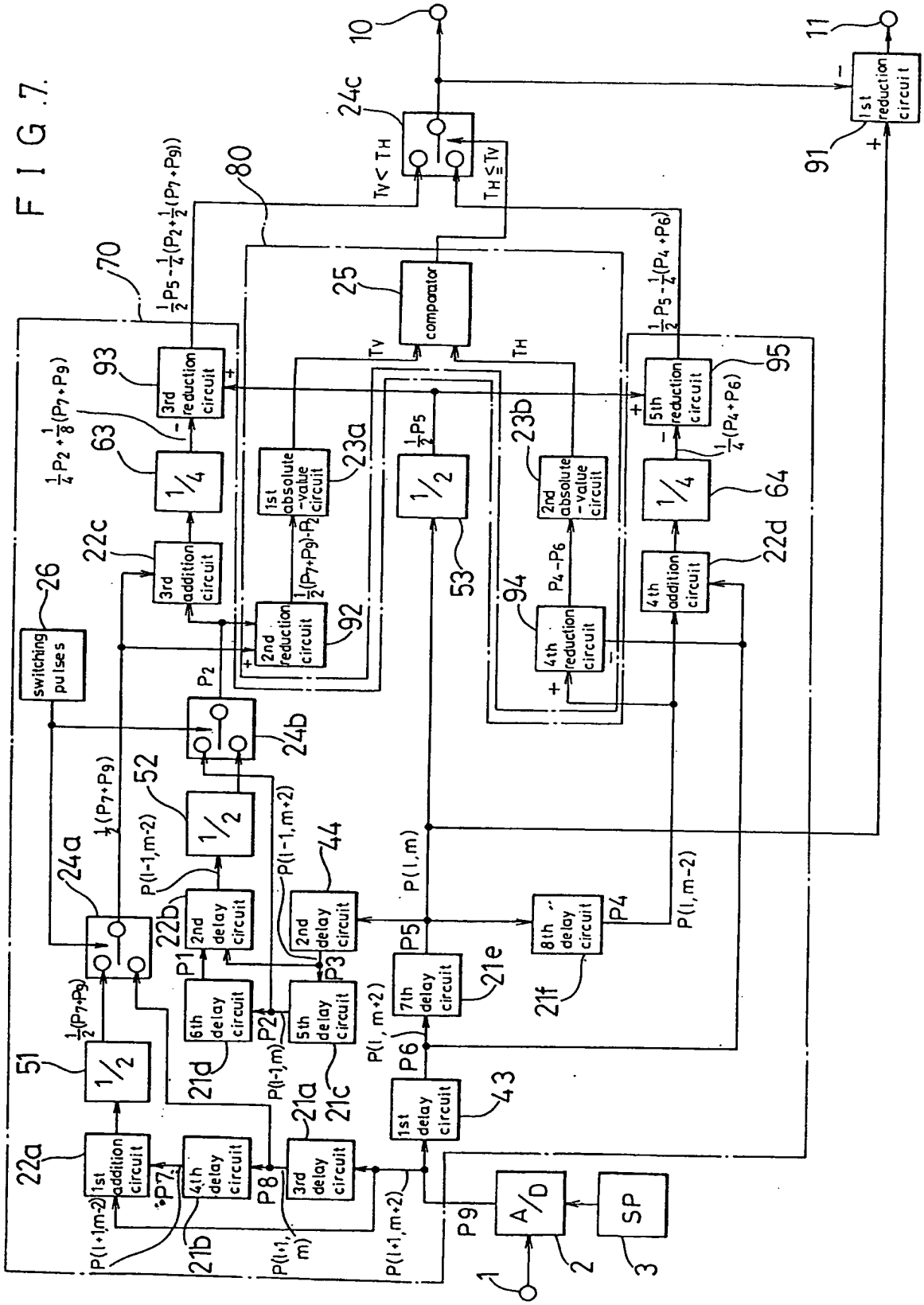

1st addition circuit
1st delay circuit
2nd delay circuit
3rd delay circuit
4th delay circuit
5th delay circuit
6th delay circuit
7th delay circuit
8th delay circuit
1st reduction circuit
2nd reduction circuit
3rd reduction circuit
4th reduction circuit
5th reduction circuit
1st absolute -value circuit
2nd absolute -value circuit
3rd addition circuit
4th addition circuit
comparator
switching pulses
A/D
SP
1/2
1/4

FIG.8.

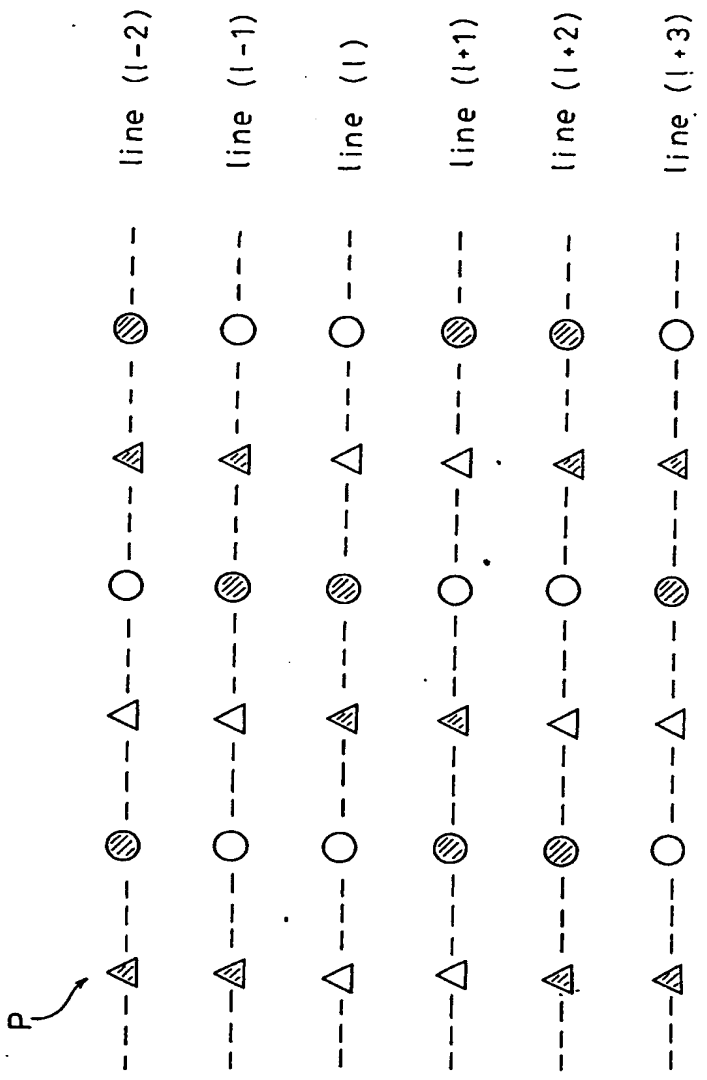

P
line (l-2)
line (l-1)
line (l)
line (l+1)
line (l+2)
line (l+3)
○ : Y+C1 ◎ : Y-C1 △ : Y+C2 ▲ : Y-C2
C1=U1+V1 , C2=U2+V2

FIG.9.

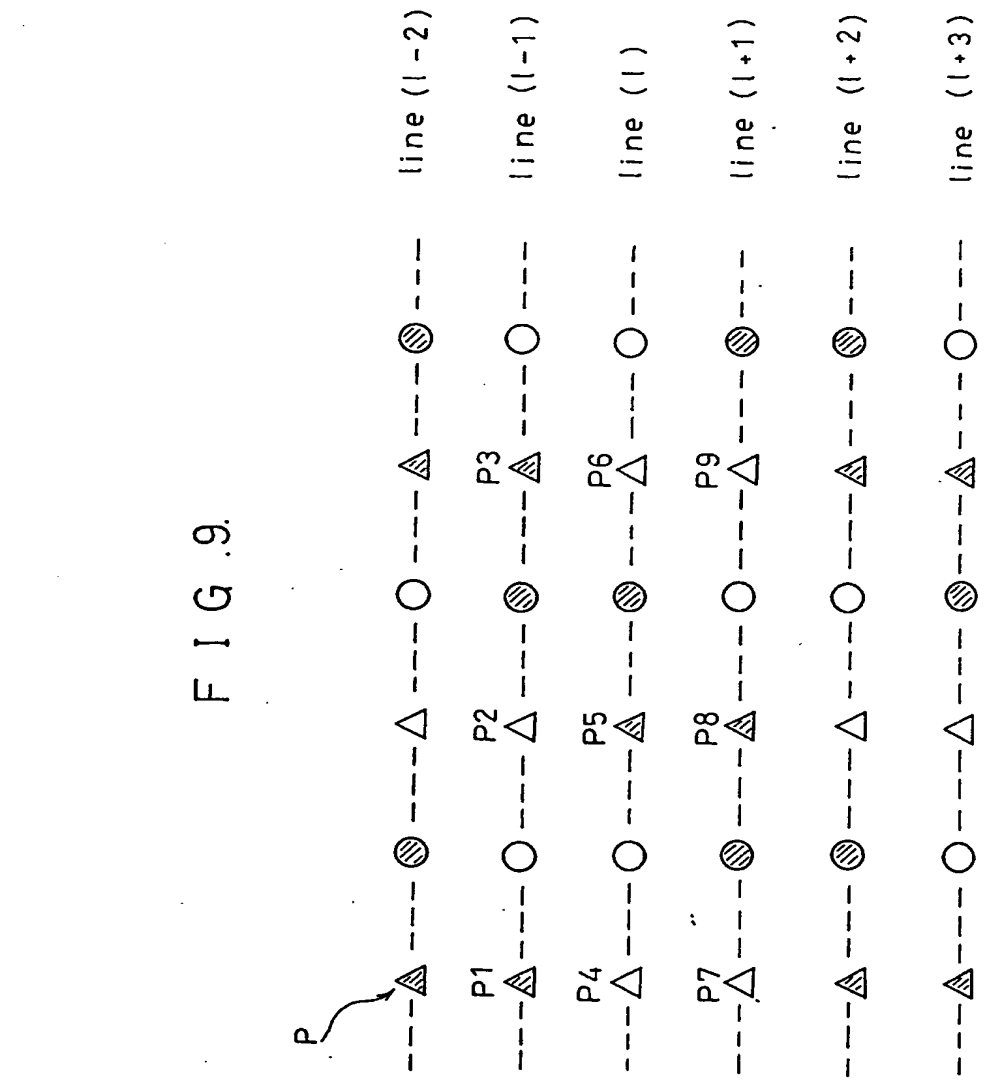
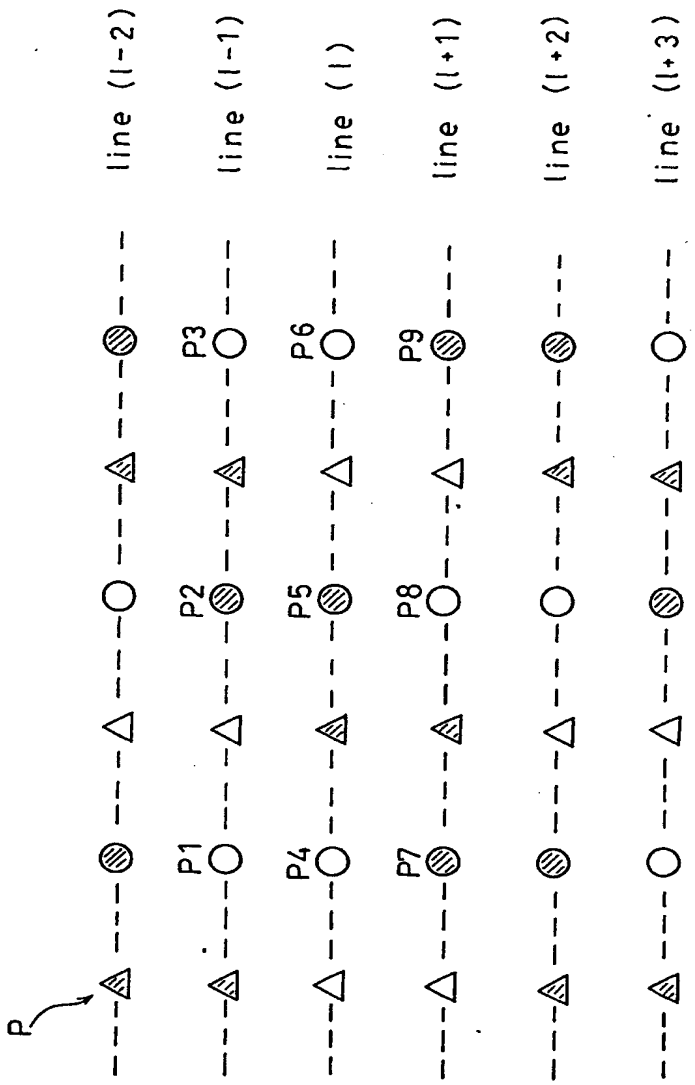

P
P1
P2
P3
P4
P5
P6
P7
P8
P9
line (l-2)
line (l-1)
line (l)
line (l+1)
line (l+2)
line (l+3)

FIG.10.


P
P1
P2
P3
P4
P5
P6
P7
P8
P9
line (l-2)
line (l-1)
line (l)
line (l+1)
line (l+2)
line (l+3)